



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: J. Fuller et al

Group Art Unit: : Endicott Interconnect Technologies, Inc.
Examiner: : IP Law, FBU/257-2 AA12
Serial No.: : 1701 North Street
Filed: Herewith : Endicott, New York 13760
Title: Circuitized Substrate Assembly And
Method of Making Same
Assistant Commissioner For Patents

Washington, D.C. 20231

Dear Sir:

INFORMATION DISCLOSURE STATEMENT/CERTIFICATION

For ensuring compliance with Applicant's/Applicants' duty of disclosure under 37 CFR § 1.56, the undersigned hereby submits the documents listed on the attached Form PTO-1449 for consideration by the Examiner in charge of the above-identified patent application.

The listing of these documents is not to be construed as an admission that such is actually prior art with respect to the invention of the present application and is not to be construed that such is material with respect to the present invention.

[] U.S. patent applications which Applicant/Applicants considers/consider to be related to the above-identified application.



- ☐ A concise explanation of the relevance of the non-English language documents is attached:
- ☐ The relevance of the documents is indicated on the enclosed copy of the _____ Search Report for the priority application _____.

These documents are being submitted (check only one of the next four boxes):

- ☒ within three months of the filing of the above U.S. national application or of the date of entry of the U.S. national stage in an International Patent Application (no fee is due);
- ☐ before receiving a first Office Action on the merits of the above-identified patent application (no fee is due);
- ☐ following receipt of a first Office Action, but before issuance of a Final Office Action or a Notice of Allowance (if this box is checked, the fee box below or one of the last two boxes must be checked);

OR

- ☐ following receipt of a Notice of Allowance or a Final Office Action (if this box is checked, the fee box and one of the last two boxes also must be checked).

CERTIFICATION

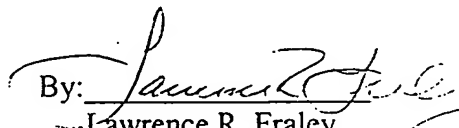
- [] The undersigned certifies that each item of this information is being submitted within three months of the date it was first cited in any communication from a foreign patent office in a counterpart foreign application.
- [] The undersigned certifies that no item of information contained in the information disclosure statement was first cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the undersigned, after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR § 1.56(c) more than three months prior to the filing of this information disclosure statement.

The Commissioner/Assistant Commissioner is hereby authorized to charge payment of any deficiency in the above fee(s) or to charge any additional fees required under 37 CFR § 1.16 or 1.17 or credit any overpayment to Deposit Account No. _____.

A duplicate copy of this authorization is included herewith.

Respectfully submitted,

Dated: Dec. 15, 2002
Telephone: 607-755-3207
Fax: 607-757-1156

By: 
Lawrence R. Fraley
Attorney for Applicant/Applicants
Reg. No. 26,885

37 CFR 1.501 INFORMATION DISCLOSURE CITATION IN A PATENT (Use several sheets if necessary)				Docket Number (Optional) EI-2-02-001		Patent Number	
				Applicant J. W. Fuller, Jr., et al			
				Issue Date		Group Art Unit	

U.S. PATENT DOCUMENTS												
EXAMINER INITIAL	DOCUMENT NUMBER						DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE	
	4	6	1	2	0	8	3	09/86	Yasumoto et al			
	5	9	0	2	1	1	8	05/99	Hubner			
	5	9	5	6	8	4	3	09/99	Mizumoto et al			
	6	3	8	8	2	0	4	05/02	Lauffer et al			
	6	4	5	9	0	4	7	10/02	Japp et al			
	6	4	7	9	0	9	3	12/02	Lauffer et al			

FOREIGN PATENT DOCUMENTS												
	DOCUMENT NUMBER						DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
											YES	NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)	
	IBM TDB, "Automatic Method For Registration And Stacking of Laminates", by Hollis
	IBM TDB, "Multilayer Subsurface Circuit Board Constructions", by Mace

EXAMINER	DATE CONSIDERED
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